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A Texas Instruments Application Report

MOSFET fm tuner design

MOSFET FM TUNER DESIGN

By
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INTRODUCTION

Dual-gate MOSFETs in an FM tuner provide many advantages over bipolar, junction field-effect, and single-gate MOS field-effect transistors. RF amplification and mixing are aided by use of a low-feedback-capacitance transistor with low noise figure and large dynamic range. A second gate is available for either AGC or local oscillator injection. High, stable RF and conversion gains are easily obtained with inexpensive, commercially available coils and without need for neutralization. This report presents test data and design tips which can be used to design with the *3N201 dual-gate MOSFET at 100 MHz. The 3N201 is an N-channel, depletion mode, dual-gate, MOS transistor with integral back-to-back zener diodes between both gates and the source to eliminate the need for special precautionary handling procedures.

100-MHz RF AMPLIFIER

DC CONSIDERATIONS

Figure 1 shows some typical 3N201 device data. It is noted in Figure 1c that for the highest Gate-1-to-drain transconductance, Gate-1-to-source (V_{G1S}) voltage should be 0.5 volts. Figure 1e indicates nearly flat transconductance for Gate-2-to-source voltage (V_{G2S}) of 4 volts and above. (A resistance should be placed in series with Gate 2 to limit excessive gate zener current caused by accidental application of V_{G2S} voltages above the typical internal zener voltage of ±12 volts.) To insure that the device is operated within its rated 450 mW, V_{G1S} should not exceed 0 volts with $V_{G2S} = 4$ volts and a 15-volt supply voltage. Operation of the device at I_{DSS} or $V_{G2S} = 4$ volts, $V_{G1S} = 0$ volts, $V_{DS} = 15$ volts, and $T_A = 25°C$, will be discussed later.

Biasing the MOSFET at I_{DSS} may pose a power supply regulation problem. From Figure 1g, a unit-to-unit total spread of from 5 mA to 30 mA can be expected. This high current can be the cause of some troublesome ground loops and unwanted oscillator pulling with AGC action. A suitable solution is the use of self-bias. Superimposed onto Figure 1g is a load line drawn to represent a 270-ohm source resistor and a 1.3-volt Gate-1-to-ground voltage. The obvious purpose of this combination is to reduce the steady-state bias current variation from 25 mA to 5 mA and to bias the typical I_{DSS} device at 1/2 I_{DSS}.

*3N201 is a special device fabricated by Texas Instruments Incorporated, Dallas, Texas.

GAIN AND STABILITY CONSIDERATIONS

The typical 3N201 100-MHz parameters are shown in Figures 1a through 1c. The reverse transfer admittance is too small to measure on the General Radio admittance bridge. Instead, a Boonton capacitance bridge was used to measure the 1-MHz reverse transfer capacitance, C_{rss}. Further inspection of this data reveals that at 100 MHz the input and output conductances are too small to measure accurately. This makes an accurate design on paper very difficult, if not impossible, to prepare. Some insight can, however, be acquired on the problem of gain and stability by making the following assumptions (see Figures 2 and 3):

1) $Y_{rs} = j\omega\,(C_{rss} + \text{stray cap.}) = 0.022$ mmho
2) $Re(y_{is}) << G_s'$ (source conductance)
3) $Re(y_{os}) << G_L'$ (load conductance)
4) $G_s' = 1$ mmho
5) $|Y_{fs}| = 12$ mmho

Here it is assumed that the input conductance of the device is $Re(y_{is})$ and the output conductance is $Re(y_{os})$ as in the case of no feedback, Y_{rs}. A source conductance of 1 mmho was chosen to offer the best device noise figure, voltage gain from the antenna, and some mismatch to reduce skewing with AGC action. Tests have shown the device noise performance to be excellent for R_s' ranging *from 1 kΩ to 2 kΩ*. Care must be taken to shield the input circuitry from the output circuitry.

A figure of merit which can be used to estimate stability is defined by Stern[1]:

$$K = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{|Y_{12}\,Y_{21}| + Re\,(Y_{12}\,Y_{21})} \qquad (1)$$

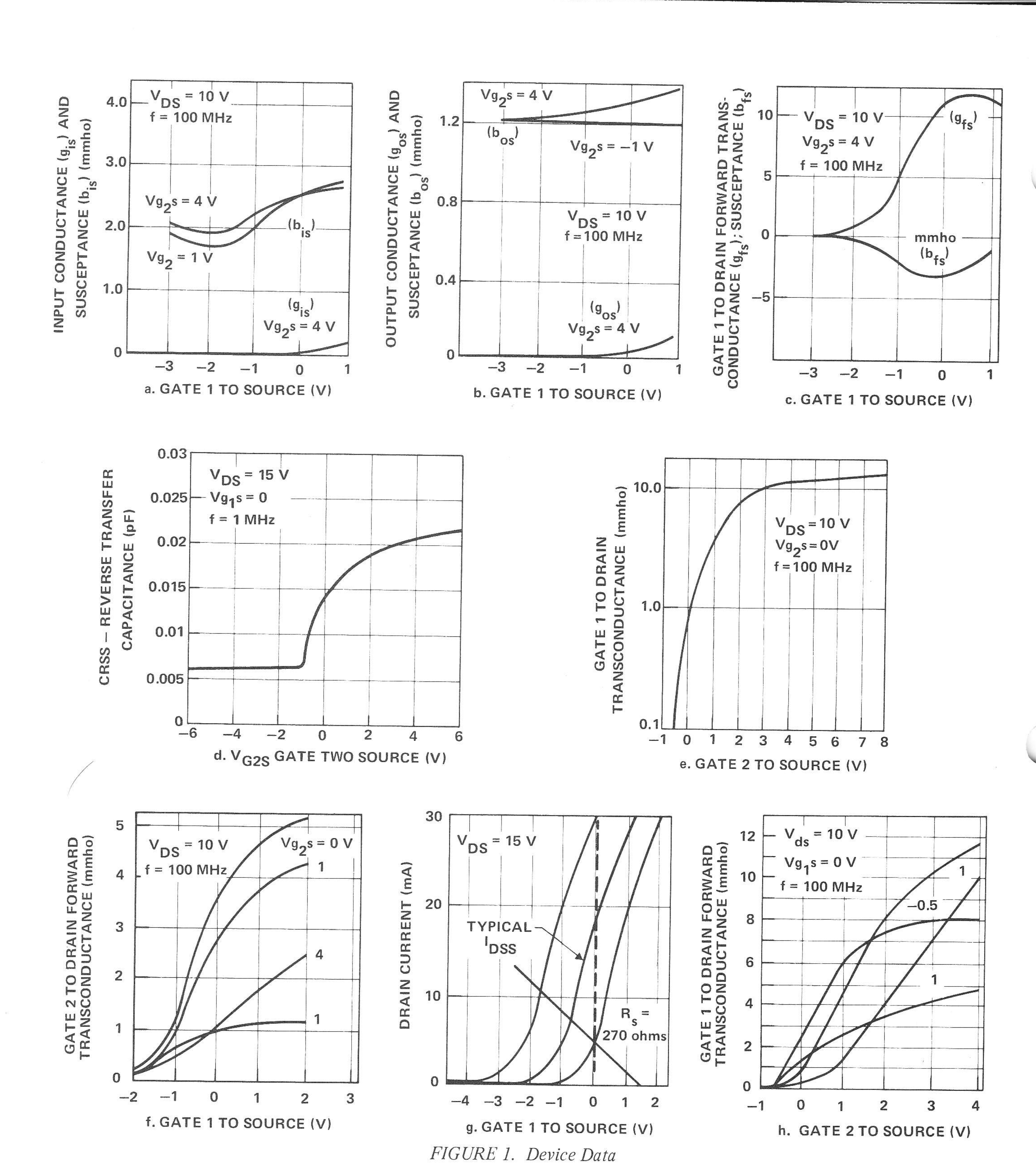


FIGURE 1. Device Data

where

K = stability factor;

$R_L' = 1/G_L'$;

$R_s' = 1/G_s'$

Solving for R_L'

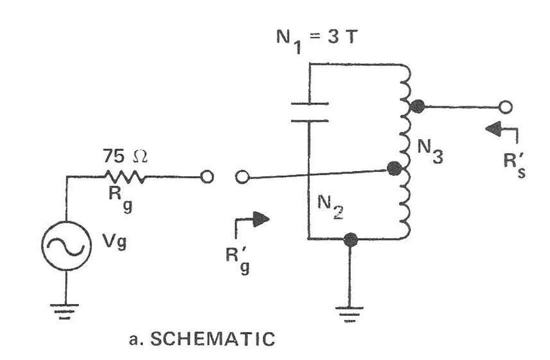
$$R_L' = \frac{2}{K R_s' \left[|Y_{12} Y_{21}| + \mathrm{Re}(Y_{12} Y_{21}) \right]} \qquad (2)$$

For K = 2, $R_L' = 4.8\ k\Omega$, and from this the voltage gain is calculated to be

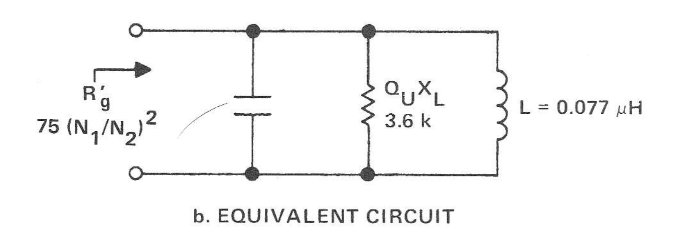
$$A_V = |Y_{fs}|\ R_L' = 57.5 \quad (3)$$

$$LVG^* = 35.2\ dB$$

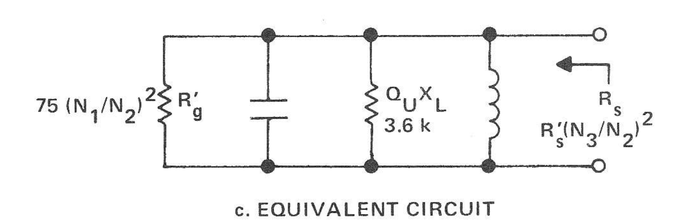
In reality this gain gave objectionable skewing in the test fixture. A more acceptable load was experimentally determined to be 2 kΩ. Therefore LVG = 27.6 dB.



a. SCHEMATIC



b. EQUIVALENT CIRCUIT



c. EQUIVALENT CIRCUIT

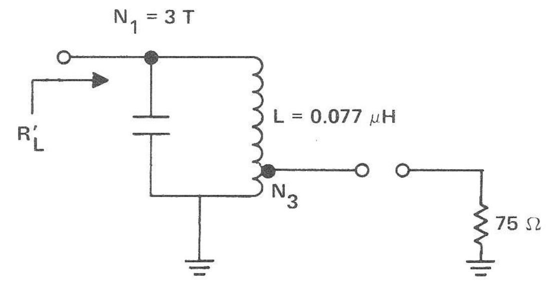
FIGURE 2. Input Coil

INPUT-COIL CONSIDERATIONS

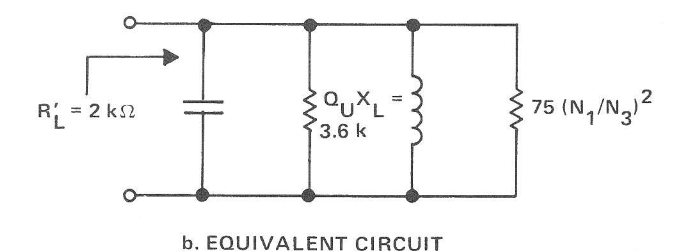
The design of the input coil can proceed with the following assumptions (see Figure 2):

1) Loaded $Q < 40$
2) $VSWR = R_g'/R_g < 2:1$
3) $Q_U = 75$
4) $X_L = 48$ ohms (0.077 μH)
5) Device input resistance neglected.

An inductance of 0.077 μH was chosen, so that a standard tuning capacitor with a delta C = 15 pF would tune the 88-MHz-to-108-MHz FM band.[2] Unloaded Q's of 75 and 140 are easily obtained by proper choice of ferrite tuning slug.



a. SCHEMATIC



b. EQUIVALENT CIRCUIT

FIGURE 3. Output Coil

The only resistance to be transformed down to match the 75-ohm antenna impedance is the coil loss $Q_U X_L$, with reference to Figure 2b,

$$(N_1/N_2)^2 = Q_U\ X_L/75 = 48 \quad (4)$$

$$N_2 = 0.434 \text{ turns}$$

$$N_1 = 3 \text{ turns}$$

With reference to Figure 2c,

$$R_s = \frac{R_g'\ Q_U\ X_L}{R_g' + Q_U\ X_L} = 1.8\ K \quad (5)$$

$$N_3 = N_1\ (R_s'/R_s)^{1/2} = 2.24 \quad (6)$$

$$Q_L = R_s/X_L = 37.5 \quad (7)$$

The coil loss, which directly contributes to noise figure, is the loaded to unloaded Q ratio.[2] For this case, $Q_L/Q_U = 0.5$ (6 dB). This is a significant degradation of noise performance. If the computations are performed again with a VSWR = 2:1 or $R_g' = 150$ ohms and an unloaded Q = 140, the new $Q_L = 36.3$ and $Q_L/Q_U = 0.26$ (−2.6 dB). The key here is relaxation of the allowable VSWR.

The input voltage gain for the first calculation is computed simply as

$$LVG = 20 \log_{10} (N_3/N_2) = 14.2\ dB \quad (8)$$

*LVG (log voltage gain) is used here to distinguish between voltage and power gain.

OUTPUT-COIL CONSIDERATIONS

Design of the output coil can proceed by making the following assumptions (see Figure 3a):

1) $40 < Q_L < 60$
2) $Q_U = 75$
3) $X_L = 48$ ohms
4) Device output resistance neglected.

From Figure 3b solving for an $R_L' = 2\ k\Omega$

$$R_L' = 75\ (N_1/N_3)^2$$

$$Q_U X_L / [75\ (N_1/N_3)^2 + Q_U X_L] \qquad (9)$$

$$N_3 = 0.387 \text{ turns}$$

$$V_g = (N_3/N_1) = 1/8\ (LVG) = (-17.8\ dB) \qquad (10)$$

$$Q_L = R_L'/X_L = 41.5 \qquad (11)$$

The total gain can now be calculated as

Gain = input + device + output

Gain = 11.8 + 27.6 + (−17.8) = 21.6 dB (12)

Note that this is power gain because both input and output impedances are the same.

With an input and output loaded Q = 40, the image frequency (100 MHz + 21.4 MHz) will be better than 50 dB down, a standard requirement of most radio manufacturers.[3]

CIRCUIT EVALUATION

This design was used as a guide to construct a test fixture. Tests were made to explore the gain characteristic, detuning of 100-MHz reference frequency, and 3-dB bandwidth changes with AGC action, as well as third-order intermodulation degradation.[4] Three circuit configurations were used (Figures 4, 5, and 6). The circuit used to take the data shown in Figures 7a through 7c was biased at $I_d = 1/2\ I_{DSS}$ and used fixed bias on Gate 1 while AGC was applied to Gate 2 only. The circuit of Figures 8a through 8d was biased at $I_d = 1/2\ I_{DSS}$ and slaved Gate 1 to Gate 2 so that Gate 1 would come down with Gate 2. The circuit of Figures 9a through 9d was biased at I_{DSS} with AGC voltage applied to Gate 2. Some points of interest are:

1) 2 dB more gain when biased at I_{DSS}
2) Biasing $I_d = I_{DSS}$ results in a 2:1 increase in frequency shift (Figures 7b and 9b), an erratic bandwidth change (Figure 9c), and a slight worsening of the intermodulation figure (Figure 9d) with AGC over the Gate 1 fixed bias condition (Figure 7c).
3) Slaving Gate 1 reduces the low-attenuation frequency shift of some devices with AGC; increases gain-reduction slope, and increases the intermodulation figure of merit of devices beyond 40 dB of attenuation.
4) The best intermodulation figure was obtained at $I_d = 1/2\ I_{DSS}$ and fixed bias on Gate 1 (Figure 7c).
5) Devices with steepest gain-reduction slopes tend to have the worst intermodulation figures.
6) The device tended to be more stable with less skewing when biased at $1/2\ I_{DSS}$.

THE MIXER

A test fixture was constructed to measure the conversion gain and $f_o + 1/2$ IF distortion for a variety of bias conditions. Data are presented for both Gate 1 and Gate 2 local oscillator injection. The mixer was similarly constructed to the RF amplifier, except that a 10.7-MHz series trap was used at Gate 1, and a tuned load of approximately 5 kΩ at 10.7 MHz.

Figures 10a and 10b contain (for the bias point) conversion power gain versus oscillator injection and f_o + 1/2 IF distortion (dB) versus oscillator injection for the case of Gate 1 injection. It is interesting to note the flatness of these curves above 600 mV rms oscillator injection. A conversion gain of 20 dB was typical, as was an f_o + 1/2 IF spurious rejection of 55 dB. The spurious test was made with no gate selectivity for a worst-case analysis. The low pinch-off devices (−2 V at 20 μA I_d) gave a gain of typically 22 dB; high pinch-off devices (−5 V at 20 μA I_d) gave gains of typically 18 dB.

Figures 10c and 10d show that, by injecting the local oscillator into Gate 2 an average conversion gain of 14 dB was observed, and 65 dB I_o + 1/2 IF spurious rejection. With the local oscillator set to 3 volts rms, spurious rejection was 68 dB. This form of injection eliminates, for all practical purposes, the interaction often observed between RF and oscillator circuits during alignment.

A complete tuner was built with injection at Gate 1 (Figure 11). Performance specifications are as follows:

Power gain	40 dB
3-dB limiting	0.9 μV
30-dB quieting	*1.5 μV
Image rejection	50 dB
f_o + 1/2 IF	80 dB
All other spurious	> 100 dB
VSWR	1.2:1

Measurements taken with a conventional four-stage IF amplifier. Test frequency, 100 MHz ± 75 kHz.

CONCLUSIONS

The dual-gate MOSFET is well suited to FM tuner service as an RF amplifier and as a mixer. As an amplifier it provides high gain, low noise, and a large AGC range

*0.7 μV with VSWR = 2:1

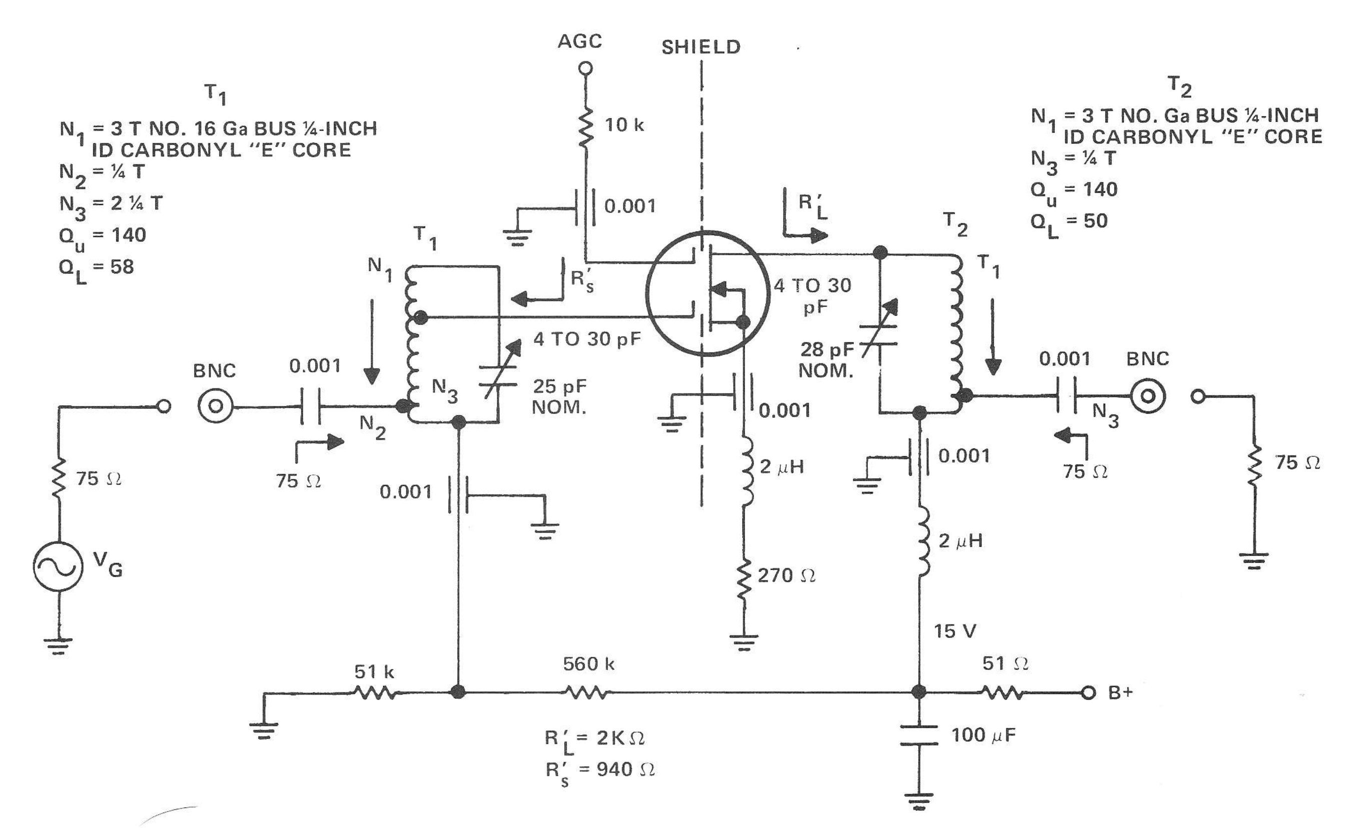


FIGURE 4. Fixed Gate 1 Bias 1/2 I_{DSS} Test Fixture

AGC
8 V TO −6 V
SHIELD
T1
N1 = 3 T 16 Ga BUS ¼-INCH ID CARBONYL "G" CORE
N2 = ¼ T
N3 = 2 ¼ T
Qu = 140
QL = 58
T2
N1 = 3 T 16 Ga BUS ¼-INCH ID CARBONYL "G" CORE
N2 = ¼ T
Qu = 150
QL = 50
10 k
0.001
R′L
R′s
T2 N1
N3
4 TO 30 pF
25 pF NOM.
28 pF NOM.
BNC
75 Ω
VG
2 μH
270 Ω
15 V
110 k
560 k
51 Ω
B+
R′L = 2 kΩ
R′s = 940 Ω

FIGURE 5. Variable Gate 1 Bias 1/2 I_{DSS} Test Fixture

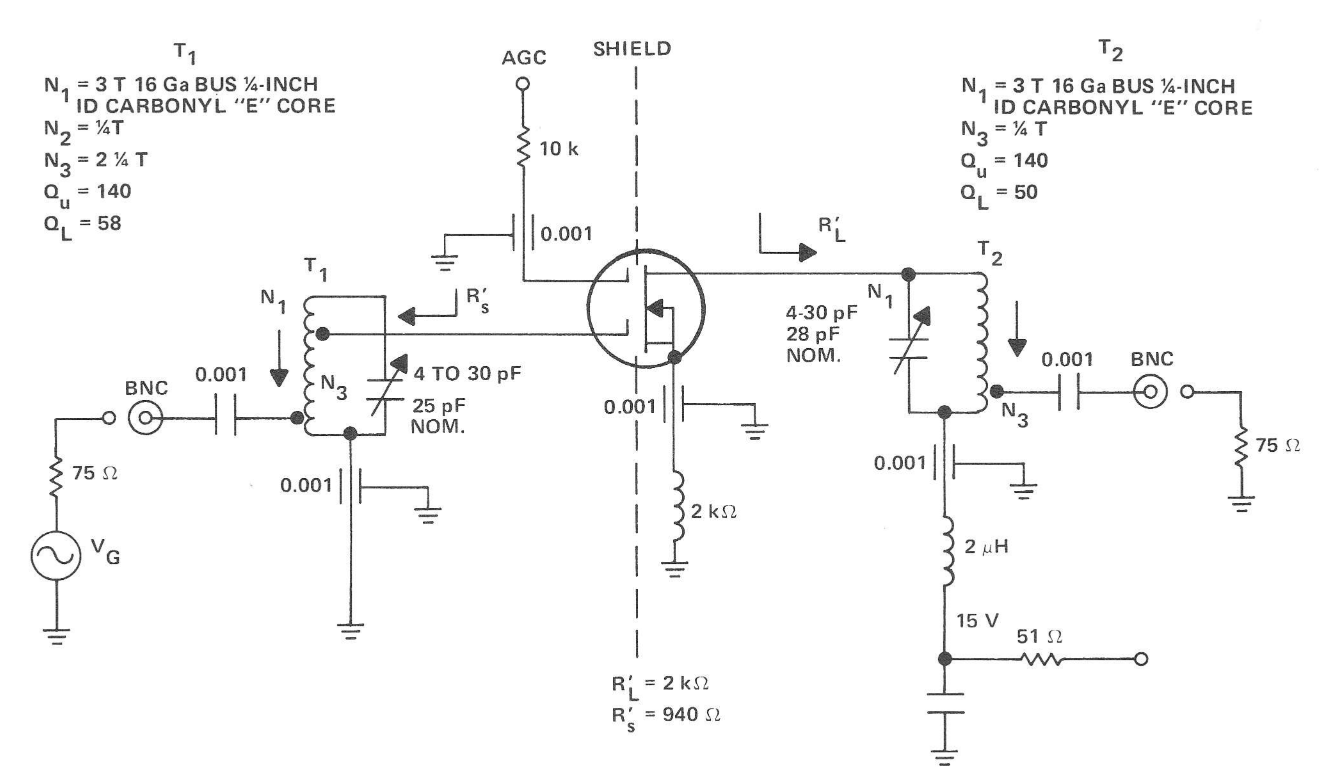


FIGURE 6. I_{DSS} Test Fixture

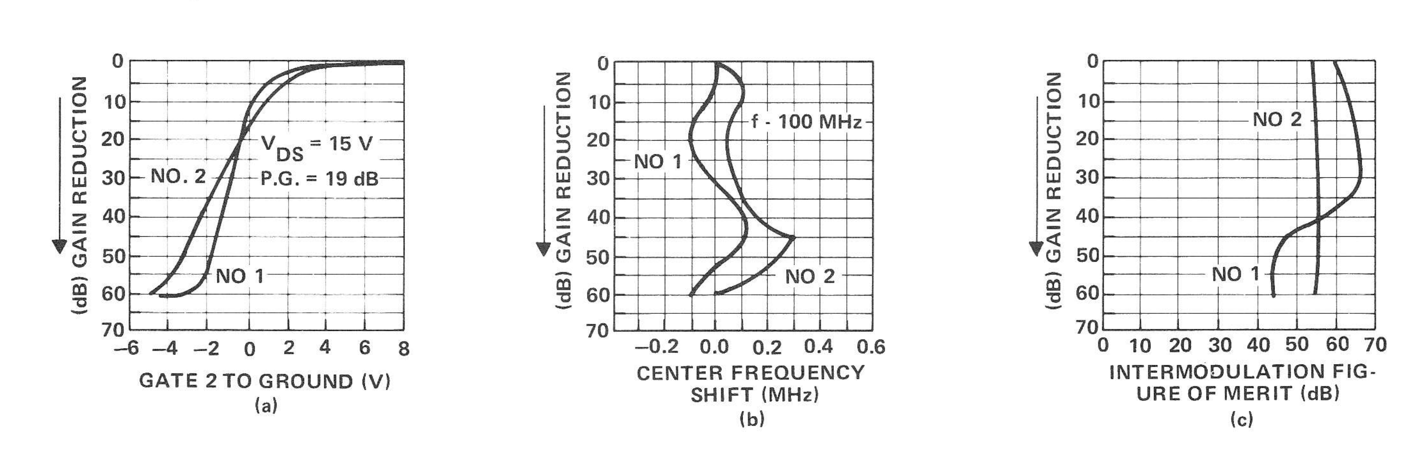


FIGURE 7. RF Performance Data with Gate 1 Fixed Biased (Schematic, Figure 4)

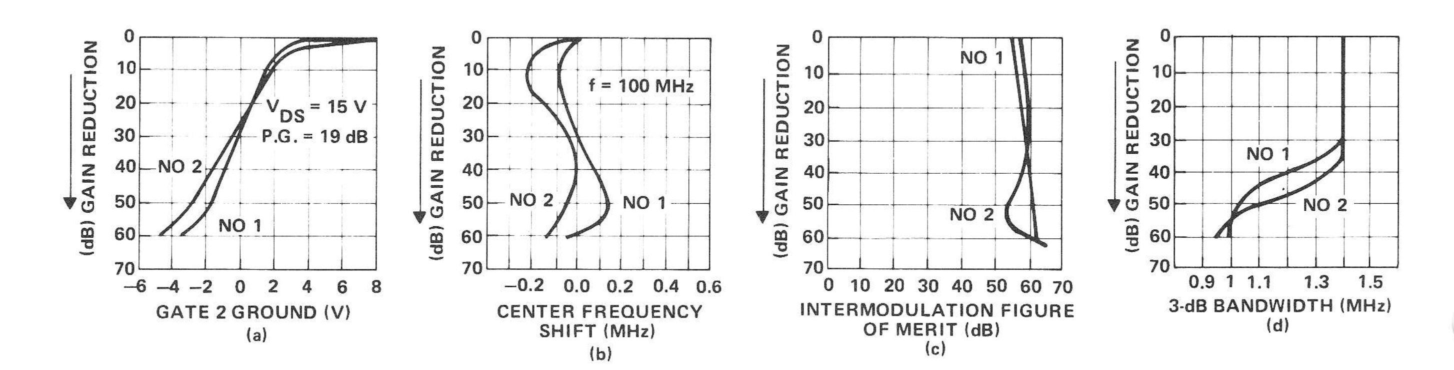


FIGURE 8. RF Performance Data with Gate 1 Slaved to Gate 2 (Schematic, Figure 5)

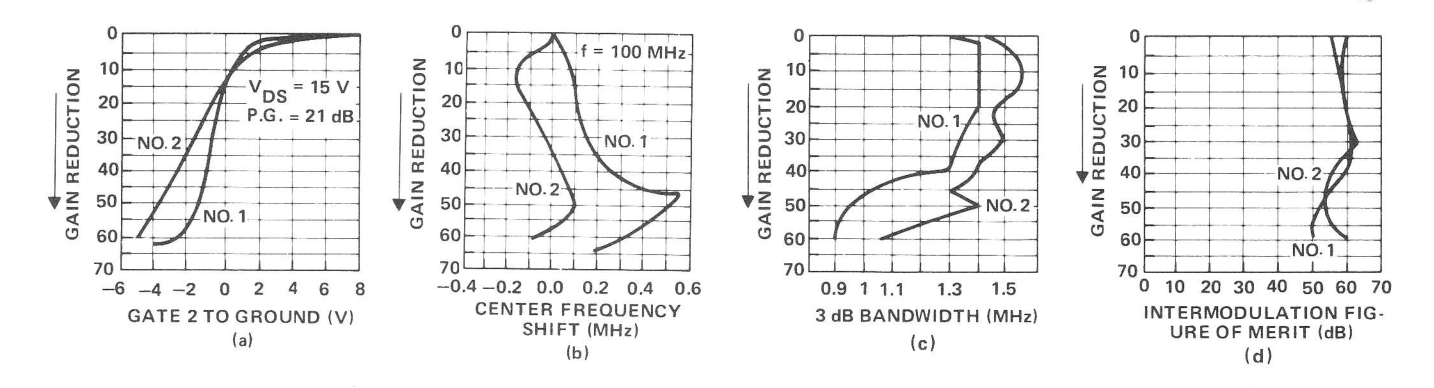


FIGURE 9. RF Performance Data Biased at I_{DSS} (Schematic, Figure 6)

FIGURE 10. Mixer Performance Data (Schematic, Figure 11)

without overload. As a mixer the dual-gate MOSFET has large conversion gain and high spurious rejection. Gate 2 L.O. injection offers 10 dB better spurious rejection but requires three times the signal. Gate 2 local oscillator injection does have an average of 6 dB less gain than Gate 1, but the gain loss necessary to eliminate all signs of RF L.O. interaction could easily make up the difference.

REFERENCES

1. Texas Instruments Incorporated, *Solid-State Communications*, New York, McGraw-Hill Book Company (1966), pp. 64-65.
2. Texas Instruments Incorporated, *Circuit Design for AM/FM, and TV*, New York, McGraw-Hill Book Company (1967), p. 113.

L1
N_1 = 3 T NO. 18 BUS, ¼ INCH ID, CARBONYL "E" CORE
N_2 = ¼ T
N_3 = 2 ¼ T
Q_u = 75
Q_L = 40

L2
N_1 = 3 T NO. 18 BUS, ¼ INCH ID, CARBONYL "E" CORE
N_2 = 2 ½ T
N_3 = 2 T
Q_u = 75
Q_L = 40

L3
N_1 = 3 T NO. 18 BUS, ¼ INCH ID, CARBONYL "E" CORE

T1
N_1 = 30 T NO. 22 Ga, CARBONYL "E" CORE
N_3 = 4 T

FIGURE 11. FM Tuner Application

3. David N. Leonard, *FM RF Amplifiers and Mixers Using Junction Field-Effect Transistors*, Texas Instruments Incorporated, Application Report (1967), pp. 7-9.
4. Ibid., p. 13.



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